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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2814	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/190,378	ALBERT, DOUGLAS M.	
	Examiner	Art Unit	
	David E Graybill	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 03 April 2000 .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) 25-27 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 and 28-32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-24 and 28-32 drawn to a process, classified in class 438, subclass 460.

II. Claims 25-27, drawn to a product, classified in class 257, subclass 458.

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process such as a process having no mechanically removing or lapping steps.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation between Joseph C. Andras and Steven H. Rao on 9-23-00 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-24 and 28-32. Affirmation of this election must be made by applicant in replying to this Office action. Claims 25-27 are withdrawn from further consideration, 37 CFR 1.142(b), as being drawn to a non-elected invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The following lack sufficient literal antecedent basis:

Claim 1, "said plurality of dies";

Claims 13, 23 and 24, "said dies";

Claims 14-16, "said die";

Claim 15, "said integrated circuit in said die";

Claim 16, "said integrated circuit on said die";

Claim 24, "a plurality of separated dies."

In claims 2, 3, 10, 18 and 19 the term "low" is a vague relative term of degree for which the disclosure provides no clear standard for measuring the degree, or it is not apparent if the degree is limited by the disclosure, and one of ordinary skill in the art in view of the prior art and the status of the art would not otherwise be reasonably apprised of the scope of the term.

In claims 2, 3, 10, 18 and 19 the term "low stress material" is vague, ambiguous and confusing because the property represented by the term is unknown. In particular, it is not clear if the term refers to an intrinsic or extrinsic property of the material or to a property externally imparted by the material to other materials.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 7-9, 13, 20, 21 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Riding (6083811).

At column 3, line 28 to column 6, line 23, Riding teaches the following:

1. A method for manufacturing a plurality of thinned integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface, comprising: defining a plurality of grooves 14 into said front surface 8 of said semiconductor wafer 10 to define said plurality of dies 20, said grooves penetrating into said surface at a predetermined distance less than said thickness of said semiconductor wafer so that said plurality of dies remain integral with said wafer; mounting said wafer to a flat rigid substrate 30 to support said wafer, said wafer being mounted to said substrate with said front surface turned toward said substrate; mechanically removing a predetermined portion of said backside 6 of said wafer until said thickness of said wafer is reduced to expose said plurality of grooves to said backside in preparation to separating said plurality of said dies, said dies remaining mounted to said substrate; and releasing said plurality of dies from said substrate.

2. The method of claim 1 further comprising disposing a planarizing layer 16 of low stress material on said front

surface of said wafer into which said plurality of grooves have been defined prior to mounting said front surface of said wafer to said flat substrate.

7. The method of claim 1 wherein defining said plurality of said grooves in said wafer comprises defining grooves approximately 50 microns deep into said front surface of said wafer.

8. The method of claim 7 wherein mechanically removing a portion of said wafer moves said backside portion of said wafer until said wafer has a thickness of 50 microns or less.

9. The method of claim 8 wherein mechanically removing a portion of said wafer removes said backside portion of said wafer until said wafer has a thickness of approximately 25 microns or less.

13. The method of claim 1 further comprising mounting said dies onto a flexible film 22.

20. The method of claim 1 where mechanically removing said wafer comprises grinding said backside portion of said wafer with at least one cycle of a predetermined grinding advance rate followed by a nonadvancing dwell.

21. The method of claim 20 where grinding with a least one advance rate and dwell comprises at least one reduction in said advance rate.

23. The method of claim 1 where defining said plurality of grooves in said front surface of said wafer comprises defining linear grooves into said front surface of said wafer in an intersecting grid pattern to define each of said dies, thereby isolating each die by a surrounding moat of stress relieving grooves.

To further clarify the teaching of defining grooves approximately 50 microns, and wherein removing a portion of the wafer removes the backside portion of the wafer until the wafer has a thickness of approximately 25 microns or less, it is noted that as cited, Riding teaches that the reduced wafer thickness is "4 mils or less," and 4 mils equals approximately 100 microns, and the claimed wafer thickness range is within this range. In addition, as cited, Riding teaches that the groove is "equal to the desired [wafer] thickness plus about 1 mil." Therefore, Riding teaches that the groove thickness is about 25-125 microns, and the claimed groove definition is within this range.

To further clarify the teaching wherein defining the plurality of grooves in the front surface of the wafer comprises defining linear grooves into the front surface of the wafer in an intersecting grid pattern to define each of the dies, thereby isolating each die by a surrounding moat of stress relieving

grooves, it is noted that this process is inherent in the teaching of Riding that "saw cuts defining the individual dice are formed in the semiconductor wafer."

To further clarify the teaching that planarizing layer 16 is of low stress material, it is noted that as cited, Riding teaches that planarizing layer 16 protects the dice from damage; therefore, it is inherent that the planarizing layer is a material having low enough stress to prevent damage to the dice.

To further clarify the teaching of a process where mechanically removing the wafer comprises grinding the backside portion of the wafer with at least one cycle of a predetermined grinding advance rate followed by a nonadvancing dwell, and where grinding with at least one advance rate and dwell comprises at least one reduction in the advance rate, it is noted that these limitations are inherent in the process of grinding and stopping grinding of Riding.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riding as applied to claims 1 and 13, and further in combination with Clifton (5480842).

Riding does not appear to explicitly teach the following:

10. The method of claim 1 wherein mounting said wafer to said flat substrate comprises affixing said wafer by means of a low viscosity low stress adhesive.

14. The method of claim 13 further comprising sealing said die mounted on said flexible film.

15. The method of claim 13 where mounting said die on said flexible film further comprises electrically coupling said integrated circuit in said die to metalizations provided on said film.

Regardless, as cited supra, Riding teaches a process wherein mounting the wafer to the substrate comprises affixing the wafer by means of a tape. Moreover, at column 3, lines 14-15; and column 4, line 51 to column 6, line 2, Clifton teaches that the wafers are "taped for protection with a low tack" adhesive. Hence, it would have been obvious to combine the process of Clifton with the process of Riding because it would facilitate mounting the wafer through the tape. Also, it is inherent in the combination that the adhesive has a stress low enough to afford protection. In addition, it would have been an

obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose a low viscosity adhesive because it would facilitate provision of a protective, low tack adhesive, and applicant has not disclosed that the viscosity is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another viscosity. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical.

Also, as cited supra, Clifton teaches a process of sealing a die 415 mounted on a flexible film 426 comprising electrically coupling an integrated circuit in the die to metalizations 421 provided on the film. Furthermore, it would have been obvious to combine the process of Clifton with the process of Riding because it would facilitate smart card fabrication.

Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riding as applied to claim 1, and further in combination with Fu (5807787).

Riding does not appear to explicitly teach the following:

3. The method of claim 1 further comprising disposing a layer of low stress material on said front surface of said wafer before defining said plurality of grooves into said front surface of said wafer.

6. The method of claim 1 further comprising disposing a polyimide layer on said front surface before said grooves are defined therein and prior to mounting to said flat substrate, so that said polyimide layer absorbs stress induced into said wafer when mechanically removing a portion of said wafer.

Notwithstanding, at column 1, lines 16-45, Fu teaches this process. Moreover, it would have been obvious to combine the process of Fu with the process of Riding because it would facilitate defining of the grooves.

Although Fu does not appear to explicitly teach that the layer is low stress, Fu teaches that the purpose of the layer is to "protect" the circuit; therefore, it is inherent that the layer is low stress.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riding as applied to claim 1, and further in combination with Poole (5162251).

Riding does not appear to explicitly teach the following:

4. The method of claim 1 where mounting said flat substrate to said front surface of said wafer comprises affixing an optically flat substrate to said front surface of said wafer.

5. The method of claim 4 where affixing said optically flat substrate comprises affixing said front surface of said wafer to a surface of said substrate which has vertical variations of approximately one micron or less across said surface.

Nonetheless, at column 3, lines 26-47; column 4, lines 46-50; column 5, line 52 to column 6, line 63; and column 7, line 51 to column 8, line 8, Poole teaches a process wherein affixing an optically flat substrate comprises affixing a front surface of a wafer shaped substrate to a surface of a substrate which has vertical variations of approximately one micron or less across said surface ("a flatness tolerance of $\lambda/2$ or better, as measured on a 1/10 wave optical flat using a monochromatic helium light source"). Furthermore, it would have been obvious to combine the process of Poole with the process of Riding because it would facilitate manufacture of thin circuits.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combinations of Riding and Clifton as applied to claim 10, and further in combination with Fu (5807787).

The combination of Riding and Clifton does not appear to explicitly teach the following:

11. The method of claim 10 further comprising disposing a polyimide layer on said front surface before said grooves are defined therein and prior to affixing to said flat substrate, so that said polyimide layer absorbs stress induced into said wafer when said grooves are mechanically formed in said wafer.

Notwithstanding, at column 1, lines 16-45, Fu teaches this process. Moreover, it would have been obvious to combine the process of Fu with the process of the combination of Riding and Clifton because it would facilitate defining of the grooves.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Riding and Clifton as applied to claim 15, and further in combination with Hayes (5681757).

The combination of Riding and Clifton does not appear to explicitly teach the following:

16. The method of claim 15 where electrically coupling said integrated circuit on said die to metalizations on said film comprises disposing said die with said front surface in contact with said metalizations on said film and coupled thereto by means of conductive epoxy.

Nevertheless, at column 10, lines 38-53, Hayes teaches a process where electrically coupling an integrated circuit on a die 96 to metalizations 86 on a substrate comprises disposing the die with a front surface in contact with the metalizations on the substrate and coupled thereto by means of conductive epoxy 92. Also, it would have been obvious to combine the process of Hayes with the process of the combination of applied prior art because it would facilitate electrical coupling of the die.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Riding and Poole (5162251).

Riding does not appear to explicitly teach the following:

22. The method of claim 21 further comprising polishing said thinned backside surface of said wafer by a dry chemical etch having an etch rate of less than one micron per minute or a mechanical polish having an advance rate of less than one micron per minute.

Although Riding does not appear to literally teach the instantly claimed "polishing," Riding explicitly teaches "grinding," and grinding is inherently polishing. Indeed, at page 11, line 20 to page 12, line 1, applicant teaches that grinding is inherently polishing.

In any case, in the alternative, at column 3, lines 25-34 and 42-46; column 4, lines 46-50; column 5, line 52 to column 6, line64; column 7, lines 10-14; and column 7, line 51 to column 8, line 8, Poole literally teaches a process of polishing a silicon substrate. Moreover, it would have been obvious to combine the process of Poole with the process of Riding because it would facilitate manufacture of thin dice.

Also, as cited, Riding teaches mechanical polishing having an inherent advance rate, and the particular claimed advance rate would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another rate. Moreover, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. Indeed, at page 12, lines 7-11, applicant explicitly discloses that the particular claimed advance rate is determined by manufacturing constraints such as the particular type of wafer grinder.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Riding as applied to claim 1, and further in combination with Cronin (5925924).

Riding does not appear to explicitly teach the following:

24. The method of claim 1 further comprising stacking a plurality of separated dies prepared by said method, and electrically interconnecting said dies.

Nonetheless, at column 10, lines 9-28, Cronin teaches this process. Moreover, it would have been obvious to combine the process of Cronin with the process of Riding because it would facilitate stacked package manufacture.

Claims 28 and 29 are rejected under 35 U.S.C. 102(e) as anticipated by Riding (6083811) or, in the alternative, under 35 U.S.C. 103(a) as obvious over the combination of Riding (6083811) and Poole (5162251).

As cited supra, Riding teaches the following:

28. A wafer dividing method comprising the steps of: forming grooves 14 in a surface 8 of a wafer 10, on which surface semiconductor elements 12 are formed, along dicing lines, said grooves being deeper than a thickness of a finished chip 20; attaching a holding member 16 on said surface of the wafer on which the semiconductor elements are formed; and lapping and polishing a bottom surface 6 of the wafer to said

thickness of the finished chip, thereby dividing the wafer into chips, wherein in the step of dividing the wafer into the chips, the lapping and polishing is continued until the thickness of the wafer becomes equal to the thickness of the finished chip, even after the wafer has been divided into the chips by the lapping and polishing.

29. The wafer dividing method according to claim 28 wherein a depth of each groove is greater than the thickness of the finished chip by at least 5 μm ("about 1 mil").

Although Riding does not appear to literally teach the instantly claimed "lapping" and "polishing," Riding explicitly teaches "grinding," and grinding is inherently both lapping and polishing. Indeed, although applicant provides no literal support in the original disclosure for the term *lapping*, at page 9, lines 21-26 of the "Request For Interference With a Patent" applicant cites the original specification at page 11, line 20 to page 12, line 1, as support for the term *lapping*, wherein applicant teaches that grinding is inherently both lapping and polishing. Similarly, applicant also provides grinding as support for lapping and polishing at page 5, lines 8-14; page 7, lines 17-19; and page 8, lines 9-13.

In any case, in the alternative, at column 3, lines 25-34 and 42-46; column 4, lines 46-50; column 5, line 52 to column 6,

line64; column 7, lines 10-14; and column 7, line 51 to column 8, line 8, Poole literally teaches a process of lapping and polishing a silicon substrate. Moreover, it would have been obvious to combine the process of Poole with the process of Riding because it would facilitate manufacture of thin dice.

Claims 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riding and the combination of Riding and Poole as applied to claims 28 and 29, and further in combination with Clifton (5480842).

As cited supra, Riding and the combination of Riding and Poole teaches the following:

31. A method of manufacturing a semiconductor device, comprising the steps of: forming semiconductor elements in a major surface 8 of a wafer 10; forming grooves 14 in said major surface of the wafer along dicing lines, said grooves being deeper than a thickness of a finished chip 20; attaching a sheet 16 on said major surface of the wafer; lapping and polishing a bottom surface 6 of the wafer to said thickness of the finished chip, thereby dividing the wafer into chips; and separating each of the divided chips from the sheet, wherein in the step of dividing the wafer into the chips, the lapping and polishing is continued until the thickness of the wafer becomes equal to the

thickness of the finished chip, even after the wafer has been divided into the chips by the lapping and polishing.

32. The method of manufacturing a semiconductor device, according to claim 31, wherein a depth of each groove is greater than the thickness of the finished chip by at least 5 μm.

However, Riding and the combination of Riding and Poole do not appear to explicitly teach the following:

30. The wafer dividing method according to claim 28 wherein said holding member comprises a substrate coated with an adhesive material.

Nor does Riding and the combination of Riding and Poole appear to explicitly teach that the sheet 16 is an adhesive sheet. Regardless, as cited supra, Clifton teaches a "low tack wafer grinding tape," and sealing each chip 20 in a package. Furthermore, it would have been obvious to combine the process of Clifton with the process of the applied prior art because it would facilitate smart card fabrication.

Claims 28-32 of this application have been copied by applicant from U.S. Patent No. 5,888,883. These claims are not patentable to applicant because they are anticipated by and unpatentable over the prior art applied supra.

An interference cannot be initiated since a prerequisite for interference under 37 CFR 1.606 is that the claim be

patentable to applicant subject to a judgement in the interference.

Claims 12 and 17-19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The prior art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show processes of manufacturing a semiconductor package similar to the process of the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the group receptionist whose telephone number is 703-308-1782.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/305-3431.

David E. Graybill
Primary Examiner
Art Unit 2814

D.G.
18-Apr-01